DATA SHEET

TDA1602A
Double-deck playback/record IC (DDPR)

Product specification
File under Integrated Circuits, IC01

April 1992

Philips Semiconductors

PHILIPS

FEATURES

- Two stereo playback preamplifiers
- Stereo playback amplifier
- High speed dubbing headswitch for channel A
- Record/playback headswitch for channel B
- Dubbing switch
- Stereo record amplifier
- Automatic level control
- Erase and bias oscillator
- Tape selector
- Reference voltage source (1/2 V_P)
- Logic part.

GENERAL DESCRIPTION

The TDA1602A is a Dolby B compatible recorder IC, which has been designed for use in double-deck recorders for Ferro/Chrome with high speed dubbing. The device performs all the basic recorder functions and needs only a very simple peripheral circuit of a few components. The DDPR may also be used in applications with automatic reverse.

All functions of the DDPR are selected by externally applied DC voltage levels. The circuit is designed for use with a mains-fed asymmetrical power supply but can also be used with a symmetrical power supply (because of its own 1/2 V_P reference voltage source).

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1602A	40	DIL	plastic	SOT129[(1)]

Note

1. SOT129-1; 1996 August 29.

QUICK REFERENCE DATA

All voltages referenced to pin 12, all currents positive into the IC

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range		7.0	–	18.0	V
Playback amplifier						
G	gain	f = 315 Hz	–	57	–	dB
S/N	signal-to-noise ratio		–	53	–	dB
THD	total harmonic distortion	V_O = 150 mV	–	0.1	–	%
Headswitch						
$V_{ON(p-p)}$	maximum voltage (peak-to-peak value)	record mode	–	–	90	V
Record amplifier						
G	gain	f = 315 Hz	–	14	–	dB
S/N	signal-to-noise ratio		–	65	–	dB
THD	total harmonic distortion	$V_{Orecord}$ = 1.5 mV	–	0.3	–	%
Automatic level control						
ΔV_O	output voltage variation	ΔV_{line} = 20 dB	–	1	–	dB
Oscillator						
f_{OSC}	frequency range		60	–	120	kHz
$I_{O(peak)}$	output current (peak value)		140	–	–	mA
$V_{O(p-p)}$	output voltage (peak-to-peak value)		–	–	36	V
Reference voltage						
V_{ref}	output voltage		–	1/2 V_P	–	V
Logic part						
I_I	input current					
	pins 8 and 10		–	100	–	µA
	pins 7 and 9		–	–	900	µA

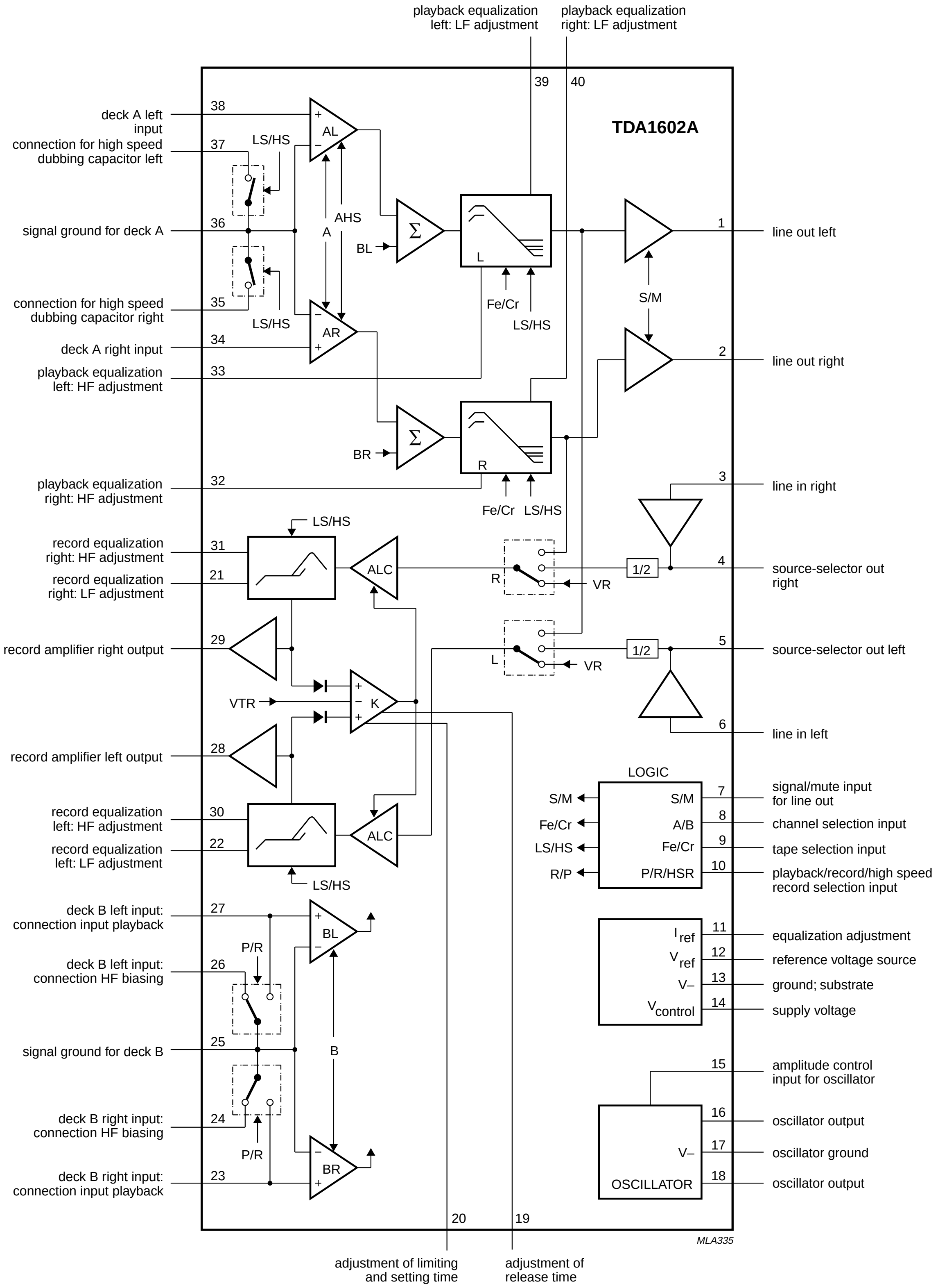


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
LOL	1	line out left
LOR	2	line out right
LIR	3	line in right
SOR	4	source-selector out right
SOL	5	source-selector out left
LIL	6	line in left
S/M	7	signal/mute input for line out
A/B	8	channel selection input
TS	9	tape selection input
P/R/HSR	10	playback/record/high-speed record selection input
EQUADJ	11	equalization adjustment
V_{ref}	12	reference voltage source
GND	13	ground; substrate
V_P	14	supply voltage
OSCCON	15	amplitude control input for oscillator
OSCO1	16	oscillator output 1
OSCGND	17	oscillator ground
OSCO2	18	oscillator output 2
ADJRT	19	adjustment of release time
ADJLST	20	adjustment of limiting and setting time
RECERLF	21	record equalization right: LF adjustment
RECELLF	22	record equalization left: LF adjustment
BRIP	23	deck B right input: connection input playback
BRIBHF	24	deck B right input: connection HF biasing
SGNDB	25	signal ground for deck B
BLIBHF	26	deck B left input: connection HF biasing
BLIP	27	deck B left input: connection input playback
RECOL	28	record amplifier left output
RECOR	29	record amplifier right output
RECELHF	30	record equalization left: HF adjustment
RECERHF	31	record equalization right: HF adjustment
PERHF	32	playback equalization right: HF adjustment
PELHF	33	playback equalization left: HF adjustment
ARI	34	deck A right input
HSDR	35	connection for high speed dubbing capacitor right
SGNDA	36	signal ground for deck A
HSDL	37	connection for high speed dubbing capacitor left
ALI	38	deck A left input
PELLF	39	playback equalization left: LF adjustment
PERLF	40	playback equalization right: LF adjustment

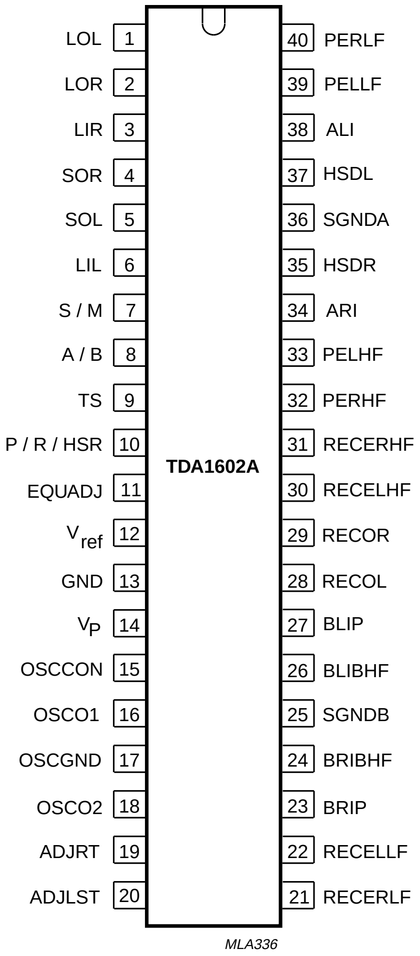


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Playback pre-amplifier

The playback preamplifier is a linear low-noise amplifier with an internal fixed gain of 26.4 dB. The relevant preamplifier for playback of channel A or B can be selected externally.

Playback amplifier

The frequency response of the playback amplifier is determined by two external capacitors (Right: C6 and C21, Left: C5 and C20). The different equalization curves for Ferro and Chrome (with time constants of 120 µs and 70 µs respectively) are controlled by the logic part of the circuit.

High speed dubbing headswitch

This electronic switch is used to connect, or disconnect, an extra external capacitor (Right: C4, Left: C1) in parallel with the gap-loss correction capacitor.

Record/playback headswitch

This is a two position electronic switch which switches the relevant side of the head to the signal ground.

RECORD POSITION

In the record mode the input of the playback amplifier is switched to the signal ground. In this way the bias and audio signal current can be applied to the head.

PLAYBACK POSITION

In the playback mode the biasing side of the head is switched to the signal ground.

Record amplifier

The frequency response of the record amplifier is determined by means of two external capacitors (Right: C11 and C12; Left: C17 and C18).

By omitting these capacitors a flat frequency response is obtained for Dolby application.

Automatic level control

The automatic level control (ALC) has a control range of 20 dB. The variation in the output voltage is less than 2 dB (see Fig.5). The attack and recovery time of the ALC can be adjusted externally.

Erase and bias oscillator

The erase and bias oscillator provides the following:

A high frequency bias current to enable a linear magnetic recording process on the tape.

A sinusoidal voltage, the amplitude of which is determined by the applied voltage at pin 15 (see also Fig.6).

The necessary current for erasing the tape which is only activated when the circuit is switched to the record mode.

Reference voltage source

This circuit delivers an output voltage which is half the supply voltage. The output voltage can be taken as signal ground. In this way a symmetrical power supply is available for the total recorder application.

Logic part

The logic part converts the incoming information from the logic input into the necessary switching signals, used in the analog parts of the circuit. The conversion is determined by the level of the input signal (see Fig.7). The logic inputs (pins 8 and 10) are independent of signal rise and fall times. The inputs at pins 7 and 9 enable smooth switching between signal/mute and Ferro/Chrome respectively.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134). All voltages referenced to pin 12; all currents positive into the IC

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	positive supply voltage		–	18	V
V_{7-10}	logic input voltage (pins 7 to 10)		0	V_P	V
V_{15}	control input voltage (pin 15)		0	V_P	V
$V_{16,18}$	oscillator output voltage (pins 16 and 18)		0	36	V
$V_{28,30}$	headswitch voltage (pins 28 and 30)		–45	+45	V
T_{stg}	storage temperature range		–55	+150	°C
T_j	junction temperature		–	+150	°C
P_{tot}	total power dissipation	T_{amb} = +60 °C	–	1.8	W

DC CHARACTERISTICS

All voltages referenced to pin 12; all currents positive into the IC; All parameters are measured in the test circuit (Fig.11) at nominal supply voltage (V_P = 15 V); f = 315 Hz; tape selectors at Fe02 position; normal speed; non-Dolby application; T_{amb} = 25 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_P	supply voltage range		7.0	–	18.0	V
I_P	supply current	note 1				
		playback mode	35	39	43	mA
		record mode	39	43	47	mA
Playback amplifier (Fe02/Cr02)						
G	gain at normal speed	f = 315 Hz	55	57	59	dB
B	frequency response with respect to gain	f = 30 Hz	10	12	14	dB
		Cr02, f = 10 kHz	–18	–17	–16	dB
		Fe02, f = 10 kHz	–13.5	–12.5	–11.5	dB
	left/right balance		–1	0	+1	dB
	A/B balance		–1	0	+1	dB
G	gain at double speed	f = 630 Hz	49	51	53	dB
B	frequency response with respect to gain	f = 60 Hz	10	12	14	dB
		Cr02; f = 20 kHz	–18	–17	–16	dB
		Fe02; f = 20 kHz	–13.5	–12.5	–11.5	dB
	left/right balance		–1	0	+1	dB
V_O	nominal output voltage	note 2; V_I = 200 μV	–	150	–	mV
THD	total harmonic distortion	V_I = 200 μV	–	0.1	0.3	%
		V_I = 280 μV	–	–	1	%
S/N	signal-to-noise ratio	note 3; weighted curve; 20 Hz to 20 kHz	51	53	–	dB
		weighted curve A(IEC179)	–	60	–	dB
	left/right separation	V_O = 150 mV	40	50	–	dB
SVRR	supply voltage ripple rejection	V_{ripple} = 100 mV; f = 100 Hz	–	25	–	dB
$\lvert Z_I \rvert$	input impedance		100	–	–	kΩ
I_{bias}	input bias current		–	0.5	–	μA
V_O	DC output voltage with respect to V_{ref} (V_{1-12} and V_{2-12})		–30	0	+30	mV
	A/B separation	note 4	–	340	–	μV
		note 5	–	tbf	–	mV
	suppression of output signal (channel A and B)	$V_7 = V_P$	–	90	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Record/playback headswitch						
$\lvert Z_{ON} \rvert$	impedance ON					
	playback mode	between pins 26 and 25 and pins 24 and 25; I = 100 μA(RMS)	–	35	100	Ω
	record mode	between pins 27 and 25 and pins 23 and 25; I = 1.5 mA(RMS)	–	25	50	Ω
I_{IL}	OFF-state leakage current	voltage on pins 24 and 26 of V_{DC} = ±45 V with respect to V_{ref} (pin 12)	–	1.0	2.5	μA
$\lvert Z_{ON} \rvert$	high-speed dubbing headswitch	normal speed, between pins 35 and 36 and pins 36 and 37; I = 100 μA(RMS)	–	100	1000	Ω
Record amplifier (ALC off)						
G	gain at normal speed	f = 315 Hz				
		note 6	13	14	15	dB
		note 7	–	20	–	dB
B	frequency response with respect to gain	f = 10 kHz	8.5	10.0	11.5	dB
		Dolby; f = 10 kHz				
		note 6	13	14	15	dB
		note 7	–	20	–	dB
	left/right balance		–1	0	+1	dB
G	gain at double speed	note 7; f = 630 Hz	19	20	21	dB
B	frequency response with respect to gain	f = 20 kHz	8	10	12	dB
	left/right balance		–1	0	+1	dB
V_O	maximum output voltage	V_{Osel} = 800 mV; f = 1 kHz; THD = 3%	–	4.0	–	V
THD	total harmonic distortion	ALC switch ON; f = 1 kHz				
		V_{Osel} = 1 V	–	–	0.7	%
		V_{Osel} = 3 V	–	0.5	–	%
S/N	signal-to-noise ratio	note 8; weighted curve 20 Hz to 20 kHz	–	60	–	dB
		weighted curve A(IEC179)	–	65	–	dB
		Dolby; weighted curve 20 Hz to 20 kHz	70	73	–	dB
	left/right separation	V_{Osel} = 300 mV	40	50	–	dB
SVRR	supply voltage ripple rejection	V_{ripple} = 100 mV; f = 100 Hz	–	30	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\|Z_I\|$	input impedance		100	–	–	kΩ
Record amplifier (ALC off)						
V_O	DC output voltage with respect to V_{ref}	normal speed record, V_{28-12} and V_{29-12}	–30	0	30	mV
R_L	load impedance on the output		10	–	–	kΩ
$\|Z_O\|$	output impedance	note 9	–	tbf	–	Ω
	suppression of line input	dubbing mode; V_{Osel} = 300 mV	–	tbf	–	dB
		deck B in playback; V_{Osel} = 300 mV	–	tbf	–	dB
Source-selector						
I_{bias}	input bias current		–	15	–	nA
S/N	signal-to-noise ratio	note 10; weighted curve 20 Hz to 20 kHz	77	90	–	dB
		weighted curve A(IEC179)	–	96	–	dB
Automatic Level Control (ALC); see Fig.5						
V_{Iref}	input reference voltage for ALC start operation		–	300	–	mV
V_{Oref}	output reference voltage	ALC switched ON; V_{Osel} = 300 mV	1.35	1.5	1.65	V
ΔV	output voltage variation	V_{Osel} = 330 mV				
		ΔV_{Osel} = 10 dB	–	0.2	1	dB
		ΔV_{Osel} = 20 dB	–	1	–	dB
t_l	limiting time	ΔV_{Osel} = 10 dB	–	1	–	ms
t_s	setting time		–	2	–	ms
t_r	release time		–	10	–	s
Erase and bias oscillator						
f_{OSC}	oscillator frequency	note 11	–	80	–	kHz
$I_{O(p-p)}$	maximum output current pins 16 and 18 (peak-to-peak value)		140	–	–	mA
V_{OSC}	output voltage pins 16 to 17 and pins 17 to 18 (peak-to-peak value)	V_P = 18 V	–	–	36	V
V_{15}	voltage control range	note 12	2.0	–	13.0	V
V_{OSC}	peak output voltage	see Fig.6; $V_{control} = V_P$ –8 V between pins 16 and 18	–	8.0	–	V
I_I	input current of control inputs		–	0.1	–	µA
THD	total harmonic distortion between pins 16 and 18	I_O = 80 mA	–	0.5	–	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Reference voltage source						
V_{12}	output voltage	note 13; no external load	7.25	7.5	7.75	V
ΔV_{12}	output voltage deviation	ΔI_{ref} = 1 mA	–100	–	+100	mV
Logics inputs (pins 7 to 10); see Figs 7, 8 and 9						
I_7	signal/mute input current	$V_7 = V_P$	–	–	900	μA
V_7	signal/mute input voltage					
		signal	0	–	0.3	V
		mute	6.0	–	15.0	V
I_8	input current for channel A/B selection	$V_8 = V_P$	–	100	150	μA
	input voltage for channel A/B selection					
		deck A	0	–	3.0	V
		mute	5.0	–	10.0	V
		deck B	12.0	–	15.0	V
I_9	input current for tape selection	$V_9 = V_P$	–	–	900	μA
V_9	input voltage for tape selection					
		Cr02	0	–	0.3	V
		Fe02	6.0	–	15.0	V
I_{10}	input current for mode selection	$V_{10} = V_P$	–	100	150	μA
V_{10}	input voltage for mode selection					
		playback	0	–	4.0	V
		record	6.0	–	9.0	V
		high-speed record	11.0	–	15.0	V

Notes to the characteristics

1. The supply current is measured in the test circuit without an additional load of the 1/2 V_P reference voltage source. In the record mode the tape selector is at position Cr02; the oscillator is OFF.
2. The output impedance of the output buffer is typical Z_O = 1 kΩ.
3. The signal-to-noise ratio is related to an output signal V_O = 150 mV with R_s = 1 kΩ. The circuit is switched at normal speed and the tape selector is at position Cr02.
4. Channel A is switched in the playback mode, at deck B a signal of V_I = 200 μV (f = 315 Hz) is applied. The output voltage at the playback amplifier is not measured selectively (bandwidth = 20 Hz to 20 kHz).
5. Deck B is switched in the record mode, at pins 24 and 26 a signal of I_I = 1 mA (f = 80 kHz) is applied.
6. Line input selected, measured relative to source selector output.
7. Switched in dubbing mode, measured relative to line output.
8. The signal-to-noise ratio is related to an output signal V_O = 1.5 V. The circuit is switched at normal speed.
9. Measured with f = 80 kHz and I_I = 1 mA.
10. The signal-to-noise ratio is related to an output signal V_O = 300 mV.
11. The oscillator frequency is determined by L_L and C_L and may be adjusted between 60 kHz and 120 kHz.
12. For stable oscillator operation the control voltage must be greater than 1 V.
13. The output voltage is independent of the operating mode (playback/record).

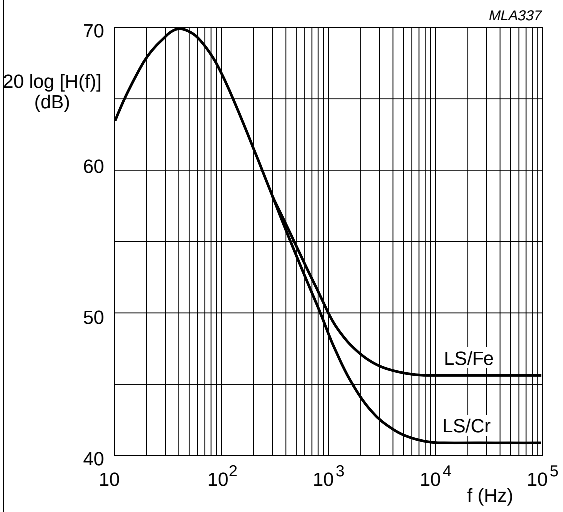


Fig.3 Typical playback frequency response.

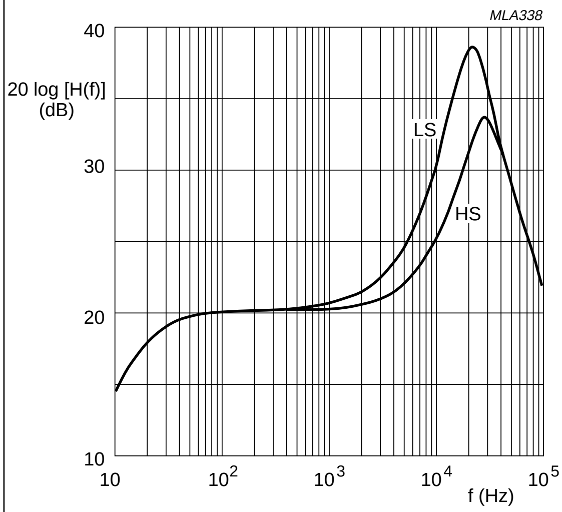


Fig.4 Typical record frequency response.

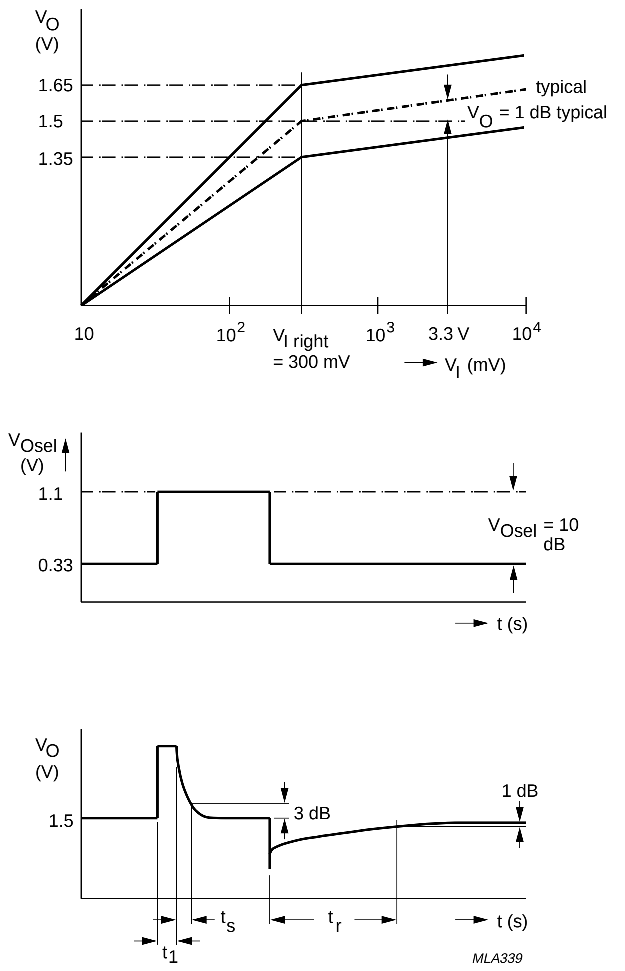


Fig.5 Typical ALC curve.

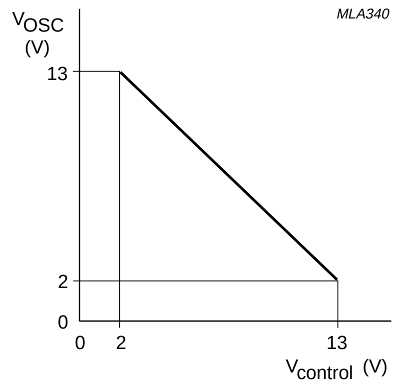


Fig.6 Control voltage/oscillator output voltage (V peak).

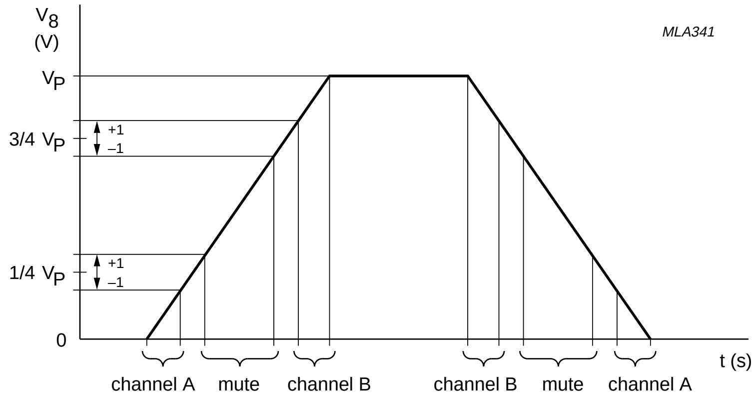


Fig.7 Channel selection input.

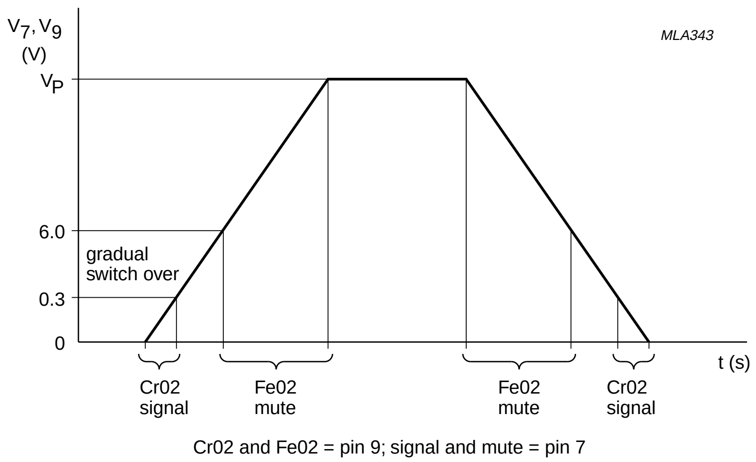


Fig.8 Tape selection input and signal/mute input.

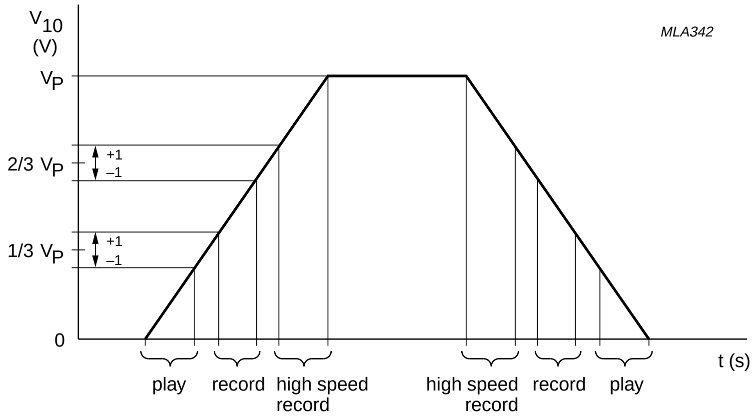


Fig.9 Playback/record/high-speed selection input.

Table 1 Logic DDPR (S/M input not included)

LOGIC INPUTS		CHANNEL	R/P	HS	Fe/Cr	PB	DUB.	REC.	ALC	BIAS
A/B	Fe/CrA	SELECT	SWITCH	SWITCH	PB	AMP.	SWITCH	AMP.	OP.	OSC.
Playback										
A	Fe	A	P	ON	Fe	ON	mute	OFF	OFF	OFF
A	Cr	A	P	ON	Cr	ON	mute	OFF	OFF	OFF
B	Fe	B	P	ON	Fe	ON	mute	OFF	OFF	OFF
B	Cr	B	P	ON	Cr	ON	mute	OFF	OFF	OFF
Record										
A	Fe	A	R	ON	Fe	ON	dubbing	ON	OFF	ON
A	Cr	A	R	ON	Cr	ON	dubbing	ON	OFF	ON
B	Fe	A	R	ON	Fe	ON	line	ON	ON	ON
B	Cr	A	R	ON	Cr	ON	line	ON	ON	ON
High speed record										
A	Fe	AHS	R	OFF	Fe	ON	dubbing	ON	OFF	ON
A	Cr	AHS	R	OFF	Cr	ON	dubbing	ON	OFF	ON
B	Fe	A	R	ON	Fe	ON	line	ON	ON	ON
B	Cr	A	R	ON	Cr	ON	line	ON	ON	ON

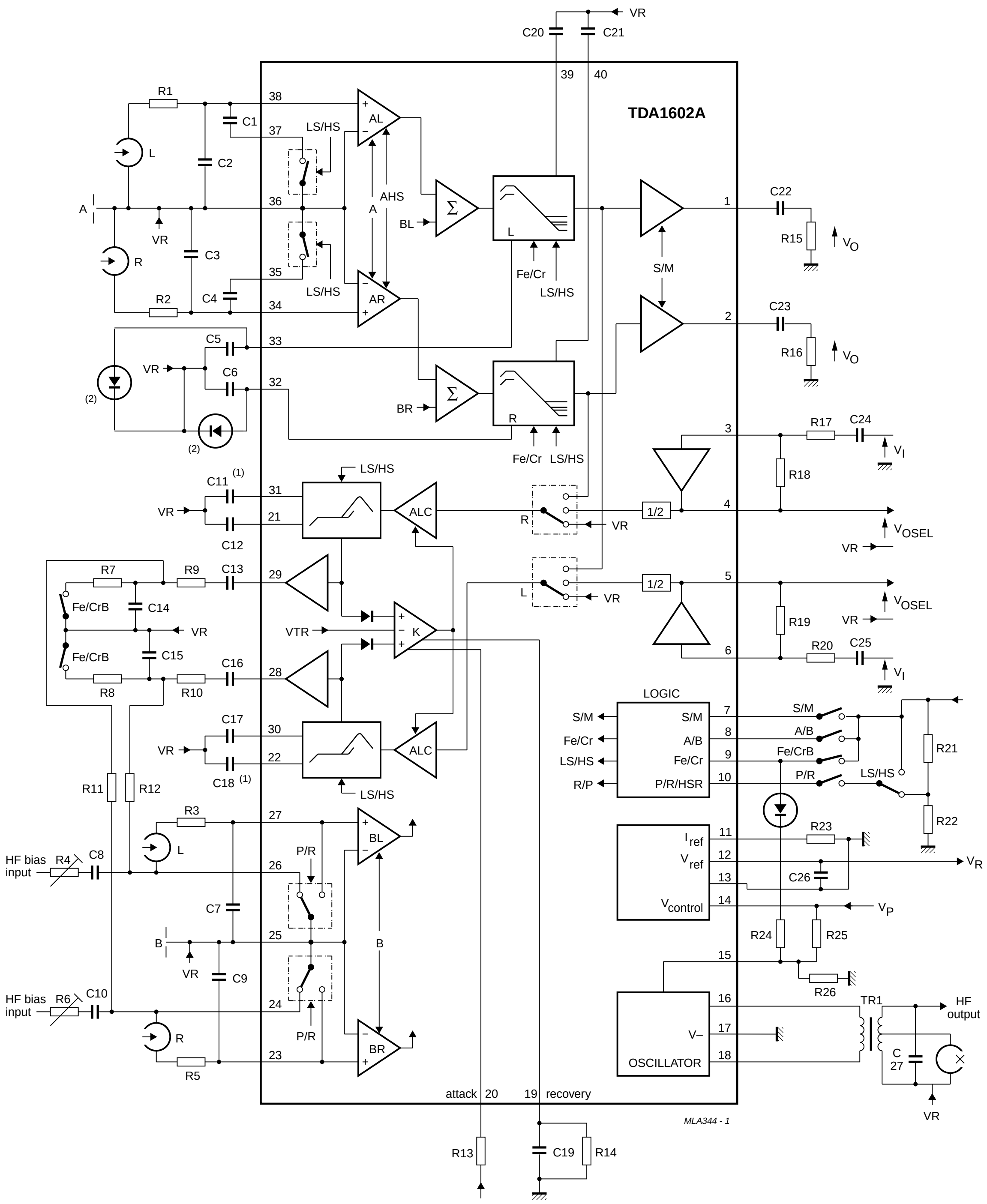
Table 2 Double deck application

DECK SELECT		A/B	S/M	CHANNEL	HS	PB	DUB.	ALC
A(P)	B(R/P)	INPUT	INPUT	SELECT	SWITCH	AMP.	SWITCH	OP.
Playback								
$\overline{A}$	$\overline{B}$	don't care	M	A or B	OFF	OFF	mute	OFF
$\overline{A}$	B	B	S	B	OFF	ON	mute	OFF
A	$\overline{B}$	A	S	A	OFF	ON	mute	OFF
Record								
$\overline{A}$	B	B	M (1)	A	OFF	OFF (1)	line	ON
A	B	A	S	A	OFF	ON	dubbing	OFF
High speed record								
$\overline{A}$	B	B	M (1)	A	OFF	OFF (1)	line	ON
A	B	A	M (1)	AHS	ON	OFF (1)	dubbing	OFF

Notes to Table 2

1. Fe/Cr selection not included.
2. S is also possible; play buffer = ON.

APPLICATION INFORMATION



(1) Dolby application: omit C11 and C18.

(2) Required for low voltage application V_P < 12 V.

Fig.10 Application diagram.

TEST INFORMATION

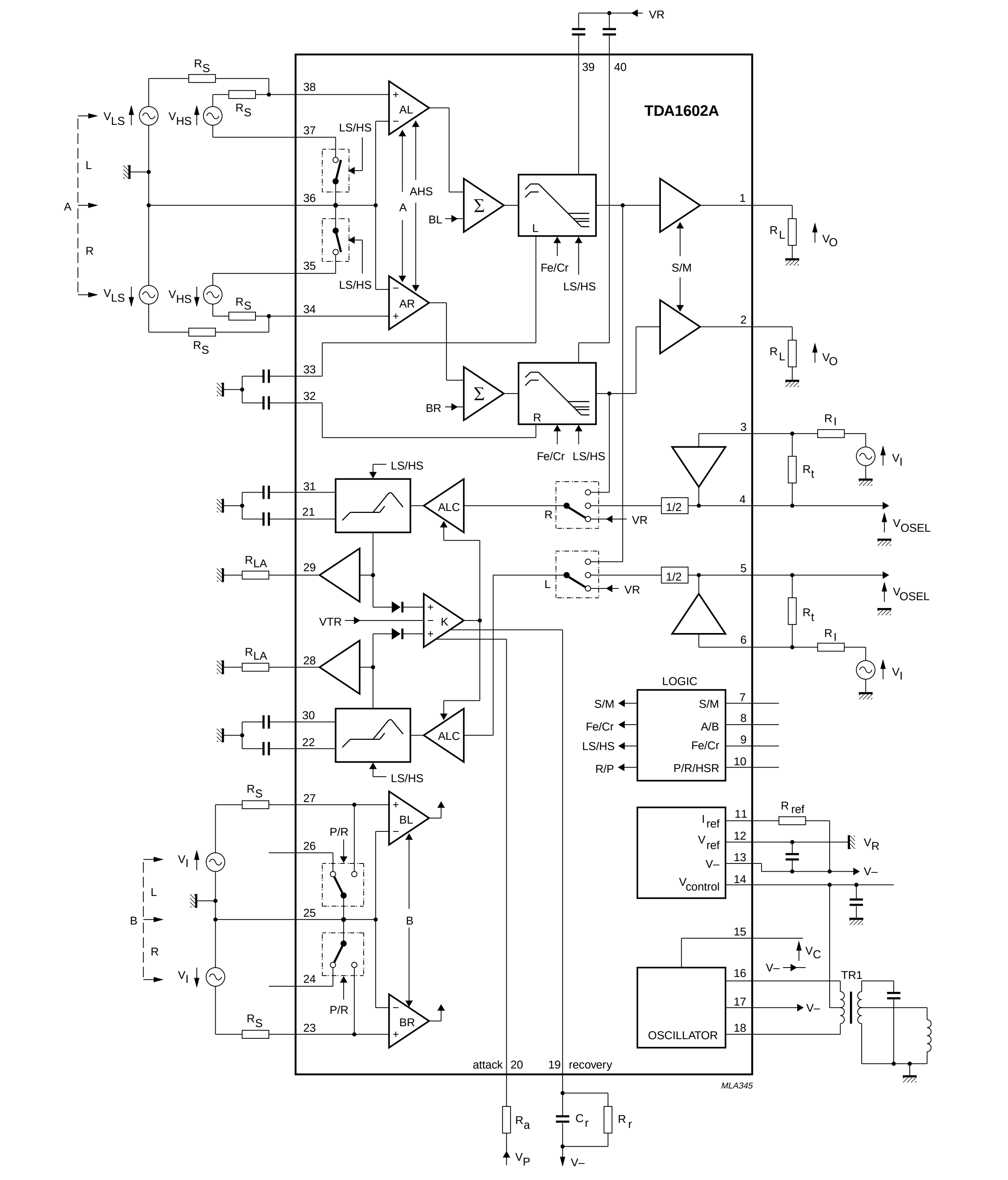


Fig.11 Test circuit diagram.

Table 3 Component values used in the application diagram

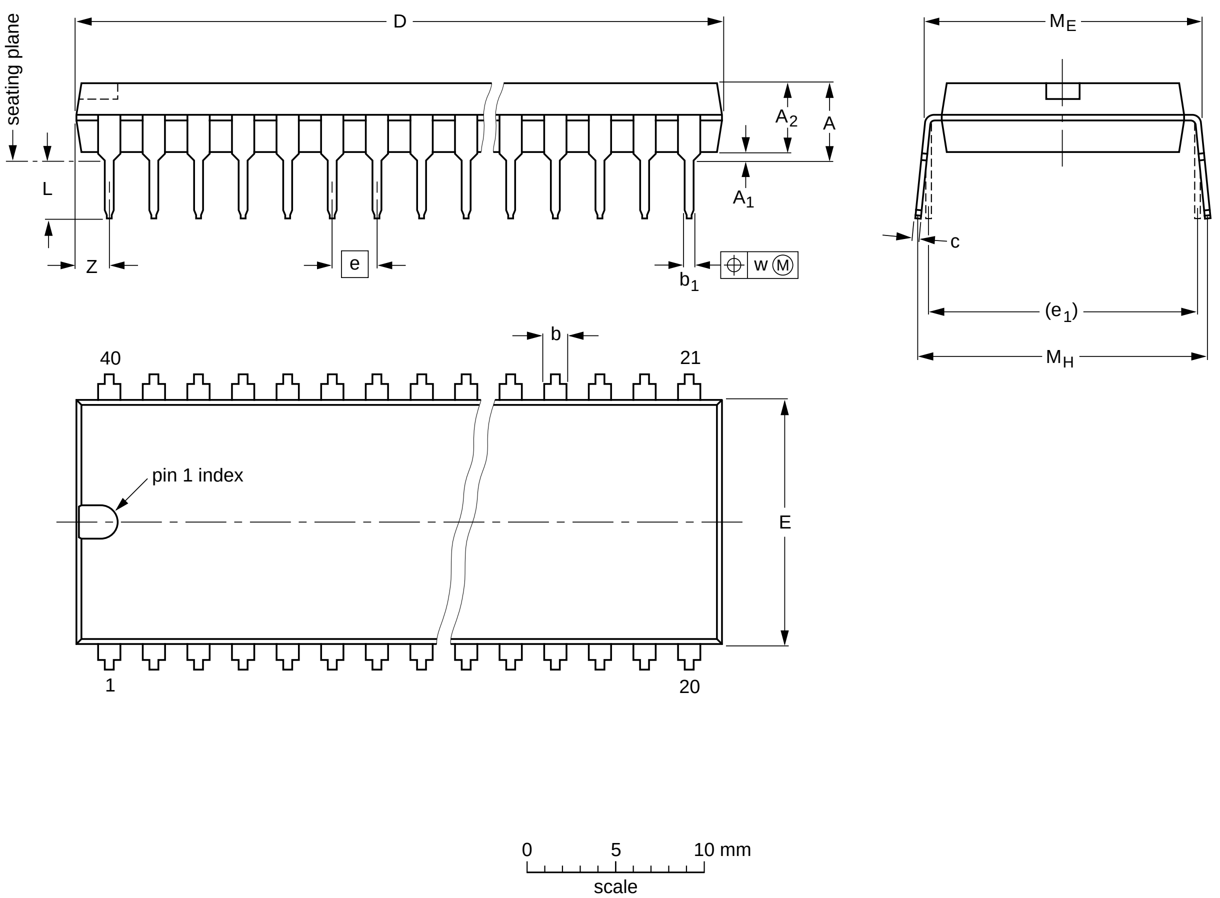
COMPONENT	CONDITION	VALUE	UNIT
Resistors			
R1, R2		47	Ω
R3, R5		47	Ω
R4, R6	potentiometer	47	kΩ
R7, R8		tbf	
R9, R10		6.8	kΩ
R11, R12		8.2	kΩ
R13		100	Ω
R14		1	MΩ
R15, R16		100	kΩ
R17, R20		tbf	
R18, R19		tbf	
R21, R22		10	kΩ
R23		2	kΩ
R24, R25, R26		5.1	kΩ
Capacitors			
C1, C4		330	pF
C2, C3		330	pF
C5, C6		47	nF
C7, C9		680	pF
C8, C10		820	pF
C11, C18		68	nF
C12, C17		100	µF
C13, C16		4.7	µF
C14, C15		tbf	
C19		47	µF
C20, C21		100	nF
C22, C23		4.7	µF
C24, C25		4.7	µF
C26		100	µF
C27		3.9	nF

Table 4 Component values used in the test circuit

COMPONENT	CONDITION	VALUE	UNIT
Resistors			
R_S		1	kΩ
R_L		100	kΩ
R_{LA}		10	kΩ
R_I		4.7	kΩ
R_t		22.6	kΩ
R_{ref}		2	kΩ
R_a		1	kΩ
R_r		3.3	MΩ
Capacitors			
C_r		1	μF

PACKAGE OUTLINE

DIP40: plastic dual in-line package; 40 leads (600 mil) **SOT129-1**

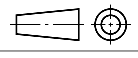


DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	4.0	1.70 1.14	0.53 0.38	0.36 0.23	52.50 51.50	14.1 13.7	2.54	15.24	3.60 3.05	15.80 15.24	17.42 15.90	0.254	2.25
inches	0.19	0.020	0.16	0.067 0.045	0.021 0.015	0.014 0.009	2.067 2.028	0.56 0.54	0.10	0.60	0.14 0.12	0.62 0.60	0.69 0.63	0.01	0.089

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT129-1	051G08	MO-015AJ				~~92-11-17~~ 95-01-14

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.